

REMARKS

No amendments, cancellations, or additions have been made to the claims of the presently claimed case. As such, claims 1-16, 19, 22-27, 29, and 30 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 103(a) Rejections

Claims 1-16, 19, 22-27, 29 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,063,689 to Chen et al. (hereinafter referred to as "Chen '689") in view of U.S. Patent No. 5,972,124 to Sethuraman et al (hereinafter referred to as "Sethuraman"). In addition, claims 1-16, 19, 22-27, 29, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,136,713 to Chen et al. (hereinafter referred to as "Chen '713") in view of Sethuraman. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond*, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). As set forth in more detail below, the cited art does not teach all limitations of the currently pending claims. Consequently, the § 103(a) rejections of claims 1-16, 19, 22-27, 29, and 30 are respectfully traversed.

None of the cited art teaches or suggests polishing a semiconductor topography to an elevation above an underlying layer using a fixed abrasive polishing process and subsequently etching portions of the semiconductor topography to expose the underlying layer. Claim 1 recites:

A method for fabricating a shallow trench isolation region, comprising blanket depositing a trench fill material over a semiconductor topography comprising one or more trenches; polishing said semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form an upper surface of the semiconductor topography at an elevation above the trenches, wherein the upper surface does not comprise a polish stop material; and etching an entirety of the upper surface simultaneously, wherein remaining portions of the trench fill material are laterally confined within the trenches.

Independent claims 12 and 22 recite similar limitations. Chen '689 and Chen '713 teach a sequence of chemical-mechanical polishing (CMP) a layer to an elevation above an underlying layer and subsequently etching remaining portions of the layer to expose the underlying layer. However, as noted in the Office

Action, neither Chen '689 nor Chen '713 teach or suggest using a fixed abrasive polishing process to planarize the topographies described therein. Sethuraman, on the other hand, does teach using a fixed abrasive polishing process to planarize a topography. Sethuraman, however, fails to teach polishing a topography to a level above an underlying layer and subsequently etching the topography to expose the underlying layer as in the presently claimed case. As such, none of the cited art anticipates the limitations of claims 1, 12, or 22.

Moreover, there is no motivation within the cited art to combine the teachings of Sethuraman with Chen '689 or Chen '713. In particular, Sethuraman specifically teaches exposing a nitride polish stop layer for the formation of a trench-filled structure. "As a result of being polished, the upper surface of trench isolation structure 56 is substantially coplanar with that of nitride layer 54." (Sethuraman, column 6, lines 48-50). In addition, Sethuraman discusses the benefits of using a fixed abrasive polishing process to polish high elevation regions without removing material from low elevation regions.

It is believed that the particles dispersed throughout the abrasive polishing surface in combination with the polishing liquid interact chemically and physically with the elevated regions of the topography to remove those regions. However, the liquid alone is believed to be incapable of removing the topography in elevationally recessed regions. Therefore, preferential removal of high elevation regions relative to low elevation regions is possible using the fixed-abrasive polishing process." (Sethuraman, column 2, lines 43-51).

Since the polishing liquid used with the fixed abrasive polishing process does not remove material from low elevation regions, the fixed-abrasive polishing process, as taught by Sethuraman, does not appear to be susceptible to dishing. Consequently, there is no motivation to alter the method of forming trench-filled structures as taught by Sethuraman. In addition, there is no motivation to modify Chen '689 or Chen '713 to polish a semiconductor topography using a fixed abrasive polishing process and subsequently etch remaining layers of the topography as in the presently claimed case.

The Office Action states that Sethuraman teaches using a fixed abrasive polishing process "in order to reduce the amount of over polishing of the Si₃N₄ polish stop ..." (Office Action, page 3). The Office Action also states that Sethuraman teaches "it is desirable to use a SiO₂ layer/ Si₃N₄ pad layer as an etch mask when forming STI trench in a CZ-Si wafer." (Office Action, page 4). Such statements are provided to support the Examiner's contention that it would be obvious to one skilled in the art to combine the teachings of Sethuraman with Chen '689 or Chen '713 to teach the limitations of the presently claimed case. It does not appear, however, that Sethuraman discusses over-polishing nitride layers and/or etching the topography described therein. Rather, Sethuraman teaches polishing an oxide layer to be coplanar with

a nitride polish stop layer and subsequently cleaning the topography to remove debris from the polishing process. As such, the aforementioned statements are asserted to be erroneous and cannot be used to support a *prima facie* case of obviousness for the presently claimed case.

For at least the reasons cited above, none of the cited art teaches or can be used to teach the limitations of claims 1, 12, or 22. Thus, claims 1, 12, and 22, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

In addition to being patentably distinct for reasons set forth above, several of the dependent claims are believed to be separately patentable for reasons set forth below.

In regard to claim 3, none of the available cited art teaches or suggests an upper surface of a shallow trench isolation region being less than approximately 200 angstroms above an upper surface of a semiconductor substrate. In fact, none of the available cited art appears to provide any teaching, suggestion or motivation to form shallow trench isolation regions having relatively small step heights, much less step heights within thicknesses that are less than approximately 200 angstroms. Without any teaching or suggestion within the cited art of forming a shallow trench isolation region to have such a step height, the limitations of claim 3 cannot be rendered obvious. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond*, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Consequently, claim 3 is asserted to be patentably distinct over the cited art.

Claims 7, 8, 10, and 11 reference different material compositions of an intermediate layer formed prior to the deposition of a trench fill material. None of the available cited art teaches or suggests layers with such materials. In particular, none of the available cited art teaches or suggests forming an intermediate layer comprising silicon carbide, carbonated polymer and/or doped oxide, such as borophosphosilicate, for example. Rather, Chen '713 and Sethuman teach forming a nitride layer and Chen '689 teaches forming a polysilicon layer prior to the deposition of a trench fill material. Without any teaching or suggestion to the materials recited in claims 7, 8, 10 or 11 to create a trench-filled structure, none of the available cited art can be used to reject the claims of the present case. As such, claims 7, 8, 10, and 11 are asserted to be patentably distinct over the cited art.

In reference to claim 9, none of the available cited art teaches or suggests forming a nitride layer with a thickness less than approximately 500 angstroms prior to depositing a trench fill material thereon. In fact, Chen '689, Chen '713 and Sethuraman do not even mention the thickness of a silicon nitride layer or the desirability to form such a layer with a thickness of less than approximately 500 angstroms for the fabrication of a trench-filled structure. As such, claim 9 is asserted to be patentably distinct over the cited art.

Claims 24-26 reference the limitation of reducing the thickness of a required layer, such as a polish stop layer, arranged under a dielectric layer. None of the available cited art even discusses the desirability to reduce the thickness of layers underneath dielectric layers. As such, none of the cited art teaches or suggests the limitations of claims 24-26, rendering them patentably distinct over the cited art.

Request for Consideration of Information Disclosure Statement

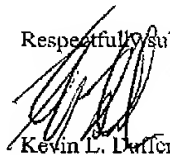
Applicant filed an Information Disclosure Statement accompanied by a Form PTO-1449 on August 8, 2001. To date, Applicant has not received notification that the references cited in the properly filed Information Disclosure Statement have been considered. Applicant hereby requests that the Examiner initial and return the Form PTO-1449 included with the Information Disclosure Statement of August 8, 2001 or indicate in some other way that the references cited therein have been considered.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed October 16, 2003. In view of the remarks traversing the rejections in the Office Action, Applicants assert that pending claims 1-16, 19, 22-27, 29, and 30 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-04700.

Respectfully submitted,



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